ARM Cortex-M0 Specifications

ARM Cortex-M0 Features	
ISA Support	Thumb® / Thumb-2 subset
Pipeline	3-stage
Performance Efficiency	1.62 CoreMark/MHz - 0.84 DMIPS/MHz (ARM Compiler version 5.0.90)*
Interrupts	Non-maskable Interrupt (NMI) + 1 to 32 physical interrupts
Sleep Modes	Integrated WFI and WFE Instructions and Sleep On Exit capability Sleep & Deep Sleep Signals Optional Retention Mode with ARM Power Management Kit
Bit Manipulation	Bit banding region can be implemented with Cortex-M System Design Kit
Enhanced Instructions	Hardware single-cycle (32x32) multiply option
Debug	Optional JTAG & Serial-Wire Debug Ports. Up to 4 Breakpoints and 2 Watchpoi

** 0.90 DMIPS/MHz using RVCT 4.0 compiler*

ARM Cortex-M0 Implementation Data**			
	180ULL (7-track, typical 1.8v, 25C)	**90LP** (7-track, typical 1.2v, 25C)	**40G** (9-track, typical 0.9
Dynamic Power	73µW/MHz	16µW/MHz	4µW/MHz
Floorplanned Area	0.13 mm^2	0.04 mm^2	>0.01 mm^2

*** Base usable configuration includes 1 IRQ + NMI, excludes debug*

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